CLAIM LISTING

The claims as listed in this claim listing replace all previous versions of the claims.

1-43. (**Canceled**)

44. (**Previously Presented**) An apparatus comprising:

a memory element directly coupled to a local memory bus, the local memory bus separate from the system memory bus, the memory element to be addressable via the system memory bus;

an on-board processor having an arbiter to arbitrate the system memory bus, including monitoring the system memory bus for a reserved memory address and issuing a control signal; and

a switch coupled to the local memory bus, the on-board processor, and the system memory bus, to receive the control signal and selectively switch the local memory bus, in response to the control signal, to the on-board processor to switch control of the memory element to the on-board processor, and to the system memory bus to switch control of the memory element to the host system.

45. (**Previously Presented**) The apparatus of claim 44, wherein the switch to switch the local memory bus to the system memory bus further comprises the switch to interconnect the local memory bus to the host system via one of multiple system memory card slots.

46. (**Previously Presented**) The apparatus of claim 45, wherein the switch to interconnect the local memory bus to the host system via one of the multiple system memory card slots comprises the apparatus to occupy a dual inline memory module (DIMM) slot, and the switch to interconnect the local memory bus to interconnect pins of the DIMM slot.

47. (**Previously Presented**) The apparatus of claim 44, wherein the selectively switch the local memory bus comprises the switch, by default, to switch the local memory bus to the system memory bus.

48. (**Previously Presented**) The apparatus of claim 44, further comprising the on-board processor to perform processing on data from the memory element if the local memory bus is switched to the on-board processor.

49. (**Previously Presented**) The apparatus of claim 48, wherein the on-board processor to perform processing comprises the on-board processor to perform hardware acceleration of a computationally intensive task to be performed on data in the memory element.

50. (**Previously Presented**) The apparatus of claim 48, wherein the on-board processor to perform processing comprises the on-board processor to perform processing on data from the memory element concurrently with a processor on the host system performing processing.

51. (**New**) A method comprising:

initializing a circuit coupled to a host system bus, the circuit having reserved memory locations and control logic, the reserved memory locations coupled to the control logic via an internal bus;

monitoring the host system bus for a signal indicating an address of one or more of the reserved memory locations; and

selectively coupling the internal bus to the host system bus to switch control of the indicated reserved memory location to the host system bus, or to the control logic to switch control of the indicated reserved memory location to the control logic, depending on whether the signal having the address is detected.

52. (**New**) The method of claim 51, wherein selectively coupling the internal bus to the host system bus depending on whether the signal having the address is detected further comprises:

coupling the internal bus to the host system bus to switch control of the indicated reserved memory location to the host system bus if the address comprises a first address; and

coupling the internal bus to the control logic to switch control of the indicated reserved memory location to the control logic if the address comprises a second address.

53. (**New**) The method of claim 52, further comprising disabling error correcting codes prior to switching control of the reserved memory location to the host system bus.

54. (**New**) The method of claim 51, wherein monitoring the host system bus comprises monitoring control, address, and data signals on the host system bus.

55. (**New**) The method of claim 51, further comprising detecting a write or a read signal indicating the address of the reserved memory location.

56. (**New**) An article of manufacture comprising a machine accessible medium having content to provide instructions to cause a machine to perform operations including:

initializing a circuit coupled to a host system bus, the circuit having reserved memory locations and control logic, the reserved memory locations coupled to the control logic via an internal bus;

monitoring the host system bus for a signal indicating an address of one or more of the reserved memory locations; and

selectively coupling the internal bus to the host system bus to switch control of the indicated reserved memory location to the host system bus, or to the control logic to switch control of the indicated reserved memory location to the control logic, depending on whether the signal having the address is detected.

57. (**New**) The article of manufacture of claim 56, wherein the content to provide instructions to cause the machine to perform selectively coupling the internal bus to the host system bus depending on whether the signal having the address is detected further comprises the content to provide instructions to cause the machine to perform:

coupling the internal bus to the host system bus to switch control of the indicated reserved memory location to the host system bus if the address comprises a first address; and

coupling the internal bus to the control logic to switch control of the indicated reserved memory location to the control logic if the address comprises a second address.

58. (**New**) The article of manufacture of claim 57, further comprising the content to provide instructions to cause the machine to perform disabling error correcting codes prior to switching control of the reserved memory location to the host system bus.

59. (**New**) The article of manufacture of claim 56, wherein the content to provide instructions to cause the machine to perform monitoring the host system bus comprises the content to provide instructions to cause the machine to perform monitoring control, address, and data signals on the host system bus.

60. (**New**) The article of manufacture of claim 56, further comprising the content to provide instructions to cause the machine to perform detecting a write or a read signal indicating the address of the reserved memory location.